LOYOLA COLLEGE (AUTONOMOUS), CHENNAI – 600 034

B.Sc. DEGREE EXAMINATION – PHYSICS

FIFTH SEMESTER – NOVEMBER 2009

PH 5501 - ELECTRONICS - I

Date & Time: 02/11/2009 / 9:00 - 12:00 Dept. No. | | Max. : 100 Marks

PART A

Answer all questions: 2 x 10 = 20 marks

1. What are hybrid parameters? Give their limitations.

2. State Norton's theorem.

3. Mention the conditions to be fulfilled to achieve faithful amplification.

4. Draw the circuit of common emitter transistor, biased using a voltage divider network.

5. Draw the circuit of an Opamp based summer.

6. Give two differences between Bipolar Junction Transistor and Field Effect Transistor.

7. Convert $(736.4)_8$ and $(F3)_{16}$ to decimal.

8. Represent NAND gate using NOR gates.

9. Give the characteristic table of RS flip flop?

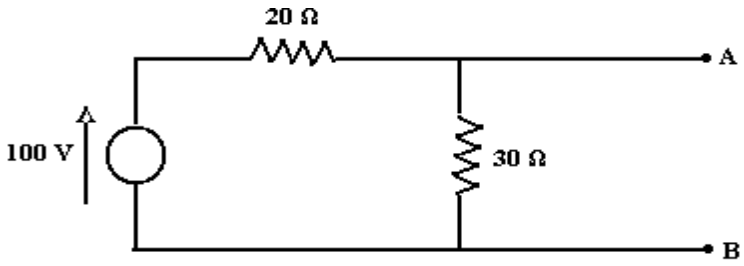
10. What is the size of a RAM with *k* address lines and *n* data input lines?

PART B

Answer any FOUR questions: 4 x 7.5 = 30 marks

11. a) State and explain Thevenin's theorem.

    b) For the two terminal network shown below, find
    (i) Open circuit voltage (ii) Thevenin resistance. (6+1.5)



12. Explain d.c and a.c load line analysis. How are they constructed on the output characteristics of a transistor? Illustrate any one.

13. a) List the characteristics of an ideal operational amplifier.
    b) Draw the schematic diagram of a non-inverting Opamp based amplifier and obtain its voltage gain. (2.5+5)

14. What is a Multiplexer? Draw the logic circuit of a 4-to-1 line multiplex and explain its operation with the function table.

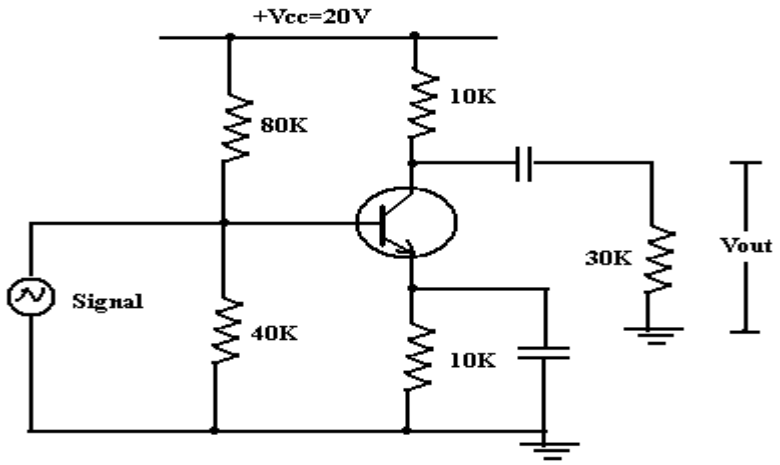
15. Explain with the logic circuit and the truth table a positive edge triggered JK flip flop. What is a master slave JK flip flop?

PART C

Answer any FOUR questions: 4 x 12.5 = 50 marks

16. a) Obtain expressions for the input impedance, current gain and voltage gain in terms of hybrid parameters for a transistor in CE arrangement.

    b) For the CE transistor amplifier shown below the h parameters of the transistor are h_{ie} = 1500Ω, h_{fe} =50, h_{re} =4x10^{-4} and h_{oe}=5x10^{-5}mho. Find (i) Input impedance, Zi looking into the base of the transistor (ii)Voltage gain, Av. (7.5+5)



17. a) Explain transistor RC coupled amplifier and discuss its frequency response.

    b) A single stage amplifier has gain of 60. The collector load Rc=500 Ω and the input impedance is 1 KΩ. Calculate the overall gain when two such stages are cascaded through R-C coupling. (10+2.5)

18. Explain the construction and working of an n- channel FET. Plot its static characteristics and state its advantages.

19. Simplify the following boolean function in both sum-of-products and product-of-sums form, using Karnaugh Map and express the results using logic diagram.
    $F(A,B,C,D)=\sum(0,1,2,5,8,9,10)$

20. Explain three bit binary ripple counter with the diagram, truth table and wave forms.

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